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EXAMINER	
HSU, JONI	

ART UNIT	PAPER NUMBER
2671	

DATE MAILED: 12/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/622,749	KARLOV, DONALD DAVID	
	Examiner	Art Unit	
	Joni Hsu	2671	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-36 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-36 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) submitted on June 6, 2005 and December 11, 2003 were filed after the mailing date of the application on July 18, 2003. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Claim Objections

2. Claim 35 is objected to because of the following informalities: Claim 35 recites the limitation "wherein said *processing unit* is a video random access memory" where applicant is assumed to have meant "wherein said *memory* is a video random access memory". Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 6-16, 18, 19, 23-29, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetter (US006342890B1) in view of Nobutani (US005613103A).

6. With regard to Claim 1, Shetter describes a method for updating the image on a computer display device, the method comprising logically dividing the computer display device into a plurality of zones (*blocks of source sub-pixels to be accessed are shifted to account for a left side bearing remainder in the final display of the character*, Col. 5, lines 1-5).

However, Shetter does not teach tracking which zones are revised and updating only the revised zones on the display device. However, Nobutani describes a method for updating the image on a computer display device, the method comprising tracking which zones are revised; and updating only the revised zones on the display device (*execute a partial rewrite of updating only the changed display data on the display screen*, Col. 1, lines 50-54).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Shetter to include tracking which zones are revised and updating only the revised zones on the display device as suggested by Nobutani because

Nobutani suggests that this increases the processing speed (Col. 1, lines 50-54; *rewrites executed for unnecessary lines lowers the processing speed*, Col. 2, lines 45-47).

7. With regard to Claim 2, Shetter describes that each zone of the plurality of zones is predefined (Col. 17, lines 50-59).

8. With regard to Claim 6, Shetter does not teach that the steps of logically dividing the computer display device into a plurality of zones, and tracking which zones are revised, are both performed by the graphical processing unit using a video random access memory. However, Nobutani describes that the steps of logically dividing the computer display device into a plurality of zones, and tracking which zones are revised (Col. 1, lines 50-54), are both performed by the graphical processing unit (213, Figure 2) using a video random access memory (212) (Col. 5, lines 40-56).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the device of Shetter so that the steps of logically dividing the computer display device into a plurality of zones, and tracking which zones are revised, are both performed by the graphical processing unit using a video random access memory as suggested by Nobutani. VRAM is a special-purpose memory used by video adapters. Unlike conventional RAM, VRAM can be accessed by two different devices simultaneously. VRAM yields better graphics performance. VRAM is well-known in the art, widely used, and can be found in many publications, such as the Webopedia Online Encyclopedia.

9. With regard to Claim 7, Shetter describes that the steps of logically dividing the computer display device into a plurality of zones (Col. 5, lines 1-5) is performed by a central processing unit (521, Figure 5A) using a system random access memory (525) (*a number of program modules may be stored on RAM 525,* Col. 7, lines 33-40).

However, Shetter does not teach tracking which zones are revised. However, Nobutani describes tracking which zones are revised (Col. 1, lines 50-54), as discussed in the rejection for Claim 1.

10. With regard to Claim 8, Shetter does not teach that the step of updating only the revised zones on the display device is performed by a graphical processing unit writing the revised zones from a video random access memory to a frame buffer. However, Nobutani describes that the step of updating only the revised zones on the display device is performed by a graphical processing unit (213, Figure 2) writing the revised zones from a video random access memory (212) to the display screen (Col. 1, lines 50-54; Col. 5, lines 40-56), and data is inherently sent to a frame buffer before going to the display screen. This would be obvious for the same reasons given in the rejections for Claims 1 and 6.

11. With regard to Claim 9, Shetter describes that the step of updating the zones on the display device (Col. 5, lines 1-5) is performed by a central processing unit (521, Figure 5A) writing the zones from a system random access memory (525, 535, Figure 5A; 535', Figure 7) directly to a frame buffer (742) (Col. 7, lines 33-40; Col. 9, line 65-Col. 10, line 2; Figure 7).

However, Shetter does not teach updating only the revised zones. However, Nobutani describes updating only the revised zones on the display device (Col. 1, lines 50-54), as discussed in the rejection for Claim 1.

12. With regard to Claim 10, Shetter does not teach that the steps of logically dividing the computer display device into a plurality of zones and tracking which zones are revised are both performed by a graphical processing unit in a video random access memory; and wherein the step of updating only the revised zones on the display device is performed by the graphical processing unit writing the revised zones from the video random access memory to a frame buffer. However, Nobutani describes that the steps of logically dividing the computer display device into a plurality of zones and tracking which zones are revised (Col. 1, lines 50-54) are both performed by a graphical processing unit (213, Figure 2) in a video random access memory (212) (Col. 5, lines 40-56); and wherein the step of updating only the revised zones on the display device (Col. 1, lines 50-54) is performed by the graphical processing unit writing the revised zones from the video random access memory to the display screen (Col. 5, lines 40-56), and data is inherently sent to a frame buffer before going to the display screen. This would be obvious for the same reasons given in the rejections for Claims 1 and 6.

13. With regard to Claim 11, Shetter describes that the steps of logically dividing the computer display device into a plurality of zones (Col. 5, lines 1-5) is performed by a central processing unit (521, Figure 5A) in a system random access memory (525) (Col. 7, lines 33-40); and wherein the step of updating the zones on the display device is performed by the central

processing unit writing the zones from the system random access memory (525, 535, Figure 5A; 535', Figure 7) directly to the frame buffer (742) (Col. 7, lines 33-40; Col. 9, line 65-Col. 10, line 2; Figure 7).

However, Shetter does not teach tracking which zones are revised and updating only the revised zones. However, Nobutani describes tracking which zones are revised and updating only the revised zones on the display device (Col. 1, lines 50-54), as discussed in the rejection for Claim 1.

14. With regard to Claim 12, Shetter describes that the method is executed in conjunction with the use of a text-enhancement technology (Col. 6, lines 24-31).

15. With regard to Claim 13, Shetter describes that the text-enhancement technology minimizes the placement errors of the sub-pixels when rounding to pixel precision (Col. 8, lines 39-58). Anti-aliasing is the technique of minimizing aliasing when representing a high-resolution signal at a lower resolution, so the text-enhancement technology is a sub-pixel anti-aliaser.

16. With regard to Claim 14, Claim 14 is similar in scope to Claim 12, and therefore is rejected under the same rationale.

17. With regard to Claim 15, Claim 15 is similar in scope to Claim 13, and therefore is rejected under the same rationale.

18. With regard to Claim 16, Shetter describes that the method is executed on a computer system that favors a system-to-video flow of data traffic, as shown in Figure 7 (Col. 8, line 59-Col. 9, line 17).

19. With regard to Claim 18, Claim 18 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

20. With regard to Claim 19, Claim 19 is similar in scope to Claim 2, and therefore is rejected under the same rationale.

21. With regard to Claim 23, Claim 23 is similar in scope to Claim 6, and therefore is rejected under the same rationale.

22. With regard to Claim 24, Claim 24 is similar in scope to Claim 7, and therefore is rejected under the same rationale.

23. With regard to Claim 25, Claim 25 is similar in scope to Claim 8, and therefore is rejected under the same rationale.

24. With regard to Claim 26, Claim 26 is similar in scope to Claim 9, and therefore is rejected under the same rationale.

25. With regard to Claim 27, Claim 27 is similar in scope to Claim 12, and therefore is rejected under the same rationale.

26. With regard to Claim 28, Claim 28 is similar in scope to Claim 14, and therefore is rejected under the same rationale.

27. With regard to Claim 29, Claim 29 is similar in scope to Claim 16, and therefore is rejected under the same rationale.

28. With regard to Claim 36, Claim 36 is similar in scope to Claim 1, and therefore is rejected under the same rationale.

29. Claims 3-5 and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetter (US006342890B1) and Nobutani (US005613103A) in view of Kusama (US006633685B1).

30. With regard to Claim 3, Shetter and Nobutani are relied upon for the teachings as discussed above relative to Claim 1.

However, Shetter and Nobutani do not teach that each zone of the plurality of zones has the same dimensions and number of pixels as the other zones. However, Kusama describes that

each zone of the plurality of zones has the same dimensions and number of pixels as the other zones (Col. 7, lines 14-21).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Shetter and Nobutani so that each zone of the plurality of zones has the same dimensions and number of pixels as the other zones as suggested by Kusama because Kusama suggests that this makes the processing of the zones more efficient (Col. 1, lines 35-39; Col. 7, lines 14-25).

31. With regard to Claim 4, Shetter describes that each zone of the plurality of zones is predefined (Col. 17, lines 50-59).

However, Shetter does not teach that each zone of the plurality of zones has the same dimensions and number of pixels as the other zones. However, Kusama describes that each zone of the plurality of zones has the same dimensions and number of pixels as the other zones (Col. 7, lines 14-21). This would be obvious for the same reasons given in the rejection for Claim 3.

32. With regard to Claim 5, Shetter does not teach that the number of zones vertically aligned on the display device is equal to the number of zones horizontally aligned on the display device. However, Kusama describes that the number of zones vertically aligned on the display device is N and the number of zones horizontally aligned on the display device is M, and gives the example of M=4 and N=5 (Col. 7, lines 8-14). However, Kusama discloses that this is only an example, and M and N can be any number, so it would be obvious for the user to modify the numbers so that they are equal to each other.

33. With regard to Claim 20, Claim 20 is similar in scope to Claim 3, and therefore is rejected under the same rationale.

34. With regard to Claim 21, Claim 21 is similar in scope to Claim 4, and therefore is rejected under the same rationale.

35. With regard to Claim 22, Claim 22 is similar in scope to Claim 5, and therefore is rejected under the same rationale.

36. Claims 17 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetter (US006342890B1) and Nobutani (US005613103A) in view of Goldberg (US005877779A).

37. With regard to Claim 17, Shetter and Nobutani are relied upon for the teachings as discussed above relative to Claim 1. Shetter describes system random access memory (525, Figure 5A) is used for logically dividing the computer display device into a plurality of zones (Col. 5, lines 1-5; Col. 7, lines 33-40).

However, Shetter does not teach tracking which zones are revised. However, Nobutani describes tracking which zones are revised (Col. 1, lines 50-54), as discussed in the rejection for Claim 1.

However, Shetter and Nobutani do not teach that this system random access memory is allocated at startup. However, Goldberg describes that the system memory used for performing an operation is allocated at startup (Col. 9, lines 14-18, 50-53).

It would have been obvious to one of ordinary skill in this art at the time of invention by applicant to modify the devices of Shetter and Nobutani so that this system random access memory is allocated at startup as suggested by Goldberg. Allocating the memory at startup means that the memory is statically allocated, which has the advantage of being fast and eliminating the possibility of running out of memory. Static allocation is well-known in the art, widely used, and can be found in many publications, such as the Memory Management Glossary.

38. With regard to Claim 30, Claim 30 is similar in scope to Claim 17, and therefore is rejected under the same rationale.

39. Claims 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Shetter (US006342890B1) and Nobutani (US005613103A) in view of Van Hook (US006675239B1).

40. With regard to Claim 31, Shetter describes a system for updating the image on a computer display device, the system comprising a memory; the memory comprising a plurality of zones (Col. 1, lines 9-15); a frame buffer (742, Figure 7) to which the processing unit (521, Figure 5A), writes zones from the memory (525, 535) to the frame buffer (Col. 6, line 65-Col. 7, line 1; Col. 9, lines 13-20, 60-63; Col. 1, lines 9-15); and a display device (547) coupled to the frame buffer, as shown in Figure 7.

However, Shetter does not teach a zone grid in the memory for tracking whether changes occur in each zone of the plurality of zones and writing only those zone that have been revised. However, Nobutani describes a system for updating the image on a computer display device, the system comprising a memory; the memory comprising a plurality of zones, a zone grid in the memory for tracking whether changes occur in each zone of the plurality of zones (Col. 1, lines 50-54); a processing unit (213, 214, Figure 2) for rendering revisions to the memory (Col. 5, lines 40-45) and tracking in the zone grid which zones of the plurality of zones are revised (Col. 5, lines 46-56); a display to which the processing unit, based on the information stored in the zone grid, writes only those zones that have been revised from the memory to the display (Col. 1, lines 50-54). This would be obvious for the same reasons given in the rejection for Claim 1.

However, Shetter and Nobutani do not teach a shadow memory in the memory. However, Van Hook describes a system comprising a memory (406, Figure 4); a shadow memory in the memory; a frame buffer to which the processing unit, writes data from the shadow memory to the frame buffer; and a display device (617, Figure 6B) coupled to the frame buffer (Col. 5, lines 58-65; Col. 6, lines 62-65).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to modify the devices of Shetter and Nobutani to include a shadow memory in the memory as suggested by Van Hook because Van Hook suggests that this reduces the amount of information that needs to be sent (Col. 3, lines 15-30).

41. With regard to Claim 32, Shetter describes that the processing unit (521, Figure 5A) is a central processing unit (Col. 6, lines 65-67).

42. With regard to Claim 33, Shetter does not teach that the processing unit is a graphical processing unit. However, Nobutani describes that the processing unit (213, 214, Figure 2) is a graphical processing unit (Col. 5, lines 40-56). This would be obvious for the same reasons given in the rejection for Claim 6.

43. With regard to Claim 34, Shetter describes that the memory (525, Figure 5A) is system random access memory (Col. 7, lines 4-6).

44. With regard to Claim 35, Shetter does not teach that the memory is a video random access memory. However, Nobutani describes that the memory (212, Figure 2) is video random access memory (Col. 5, lines 35-39). This would be obvious for the same reasons given in the rejection for Claim 6.

Prior Art of Record

"VRAM"; http://www.webopedia.com/TERM/V/VRAM.html.

"Static allocation"; p. 9; http://www.memorymanagement.org/glossary/s.html.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joni Hsu whose telephone number is 571-272-7785. The examiner can normally be reached on M-F 8am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ulka Chauhan can be reached on 571-272-7782. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JH

Kee M. Tung
Primary Examiner